Operational Guide for the GLAST ACD
High Voltage Bias Supplies (HVBS)

DAS, 5/7/04

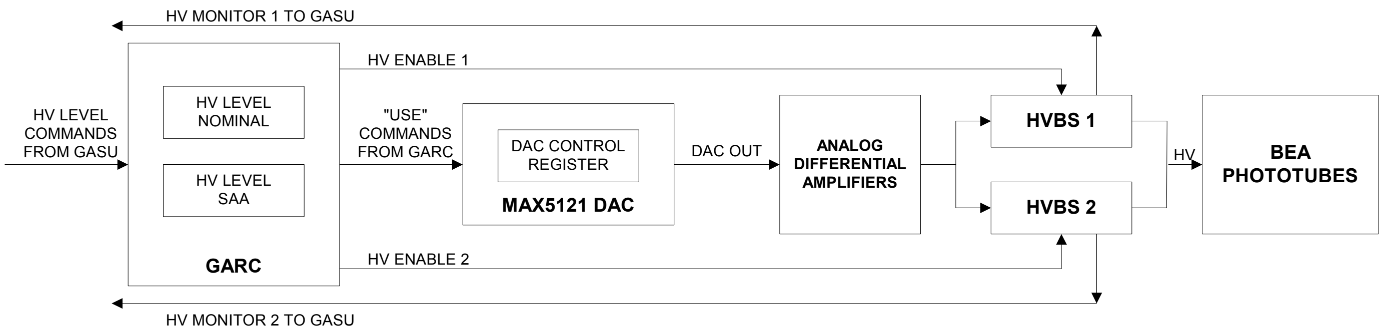
Purpose:

It is possible that the intended operation of the ACD High Voltage Bias Supplies (HVBS) and their operational constraints, including the ways these work with the BEA electronics, is not immediately intuitive. This memo seeks to document some of the design intent and explain the expected operation functions, including environmental pressure-related instrument safety issues.

Commands Associated with the ACD HVBS:

Command	Function Code	Register Number	Data Field	Comment
HV_Level_Nominal	0	8	12 bits	This is a register in the GARC that contains the 12 bit value that will be sent to the DAC with the Use HV Nominal command.
SAA_HV_Level	0	9	12 bits	This is a register in the GARC that contains the 12 bit value that will be sent to the DAC with the Use HV SAA command.
Use_HV_Nominal	0	10	N/A	This command transfers the 12 bits in the HV_Level_Nominal register from the GARC to the MAX5121 DAC.
Use_HV_SAA	0	11	N/A	This command transfers the 12 bits in the SAA_HV_Level register from the GARC to the MAX5121 DAC.
GARC_Mode	2	8	12 bit register, [11:0] bits [3:1] are HV 1Enables bits [6:4] are HV 2 Enables	These are the command bits for the Triple Modular Redundant command bits for the two supplies.
GARC_Status	2	9	N/A	This is a read-only register. Bit 1 is the HVBS 1 Enable status Bit 2 is the HVBS 2 Enable status

The block diagram below may assist operators in conceptualizing the HVBS control functions.



SIMPLIFIED BLOCK DIAGRAM OF ACD BEA HIGH VOLTAGE CONTROL

Power:

The ACD HVBS operate on +28V power supplied to the BEA through the 79 pin circular connectors. The pin locations are identical for each of these connectors. There are two HVBS per chassis assembly. The BEA receives a nominal +28V on pins 5 and 7 with the +28V_RETURN on pins 33 and 34. The HVBS cannot supply a high voltage when this power supply is off (i.e., at 0V). The FREE card uses a separate 3.3V power supply and can operate independently from the HVBS. It is important that the +3.3V FREE card power be ON when the HVBS +28V power is ON. The GARC ASIC on the FREE card must be on to ensure proper control of the HVBS enables and DAC level commands.

HVBS Control:

Once the +28V power is applied to the HVBS, the FREE board controls the output level of the supplies by means of an analog level voltage and via a digital enable level. The digital enable level is active high, meaning that +3.3V is considered ON and 0V is considered OFF. The analog level voltage is sent to the bias supplies differentially. This is controlled on the FREE card via the output of the MAX5121 Digital-to-Analog converter. The FREE card has an amplifier circuit which converts the single-ended 0 to 1.249V DAC output to a differential voltage of 0 – 2.5V with a 1.4V pedestal offset. The full range of the differential voltage (i.e., 2.5V differential) corresponds to a full-scale range on the bias supplies of approximately 1300V.

Use of Triple Modular Redundancy in the High Voltage Enable Bits:

The GARC_Mode command is used to enable and disable the two ACD HVBS in each chassis. Each HVBS is enabled/disabled independently. In the nominal operational mode, only one supply is enabled at a time.

It is considered important that the FREE electronics maintain control of the HVBS output voltages at all times. The used of Triple Modular Redundancy (TMR) in the logical constructs of the GARC seeks to alleviate the condition that a single-event upset (SEU) could alter the state of the HV Enable flip-flop. This is done by implementing a majority voting logic for these circuits. Therefore, proper use of the GARC_Mode command means that the ground command should set bits [3:1] all to the same value. This is also true for bits [6:4]. (The one exception to this would be in Functional Tests where the operation of the TMR circuitry is being checked). These GARC_Mode bits are the inputs to the TMR voting logic. The outputs of the TMR logic are the physical level signals (HV_ENABLE_1 and HV_ENABLE_2) that are passed from the GARC to the HVBS 1 and 2. The status of these levels is monitored via the read-only GARC_Status command, bits 1 and 2, respectively.

It is important that during non-operational times (e.g., periods of instrument operation when the phototubes are desired to be OFF) that these levels are controlled to the “0” or OFF state. This is the only means to keep the HVBS outputs at a zero level. If the DAC is at a “zero volts” level, but the HVBS is enabled, the flight supplies may still output over 100 V DC.

During flight operations, the GARC_Mode register values may be periodically checked to ensure no upset has occurred or should be periodically reloaded with refreshed values. A rough estimate of the GARC upset rate would indicate that once a week or once a month would be more than adequate in flight.

Operations within the South Atlantic Anomaly (SAA):

The GARC has been designed to account for proper phototube operation during SAA transitions. The SAA is a region of charged particles pulled a bit closer to the Earth’s surface by a local increase in the Earth’s magnetic field. The implication for the ACD, which is by definition a charged particle detector, is a very substantial increase in the amount of light scintillating in the tiles in this region. Due to the radiation increase, no science observations will be possible for the LAT during SAA transitions, which will occur approximately every 100 minutes (but will vary based on the procession of the LAT orbit).

If the PMT high voltage is left at nominal levels during this time, there will be excess current flowing through the tubes, resulting in a decreased lifetime of the detector system. It is desirable to decrease the PMT high voltage (which is nominally about 1000V for a gain of about 1×10^6) by several hundred volts to reduce the electron multiplication gain by several orders of magnitude. However, it is also not desirable to turn of the HVBS completely due to the mechanical stress associated with the cycling of high voltage capacitors. An intermediate approach is to maintain a level of bias on the PMTs that is represents a very low electron multiplication gain while not allowing a substantial electric field change within the high voltage capacitors. Therefore, it is more desirable to turn the PMT voltage down to a number such as 400V or 500V.

This is accomplished by having two levels stored in the GARC – a “nominal” science operations level and a lower, protected level, which is designated as the “SAA level”. These values are stored in registers in the GARC and sent to the DAC at the appropriate orbital times.

One fact about the FREE electronics that is not necessarily intuitive is that the DAC output (which becomes the differential analog level control for the HVBS) is controlled by a register in the MAX5121 DAC, not the GARC. The values stored in the GARC are loaded into the MAX5121 register whenever one of the “Use Level” commands is sent. This allows the ACD BEA operator to verify that the correct values are in the GARC registers prior to enabling transmission of the value from the GARC to the DAC.

One other advantage to this approach is refreshing the contents of the MAX5121 DAC control register. The MAX5121 is not a radiation-hardened part; it is a commercial device. A single-event upset in the control register will be reflected in the DAC output. The process of sending the “Use Nominal” and “Use SAA” commands provides an automatic memory-scrubbing cycle on this register, which is designed to mitigate the effects of SEUs on the DAC logic. Additionally, operators should note that the value written into the MAX5121 DAC may be read back just one time; this part has the curious feature of a destructive read operation. This is the only GARC-addressable register which operates in this manner.

This feature may be understood by doing a GARC Write command to one of the Use HV Level Function/Registers and then doing a GARC Read command to the same Function/Register. This will return the value from the MAX5121. Subsequent reads will produce a different data pattern; the read is destructive in nature. Reading the MAX5121 does not affect the value latched into the part, however. Only the verification aspect is destructive.

Consideration of the Pressure of the Environment in which the HVBS Operates:

The ACD HVBS are sensitive to the gas pressure under which they are operated. This is an ACD instrument safety issue. Operators of the ACD must be conscious never to enable the high voltage bias supplies unless the pressure is approximately 1 atmosphere (e.g., 760 torr nominal) or the pressure is less than 5×10^{-6} torr in a vacuum environment. If operated in a vacuum environment, the electronics should have been at the $< 5 \times 10^{-6}$ torr limit for 12 hours or more to ensure proper venting. If the HVBS are operated in between these regions (i.e., in the region 5×10^{-6} torr < Pressure < Ambient) , there is a possibility of a corona discharge occurring in either the HVBS or the PMT assemblies. (We would expect arcing when the local pressure around a HV component is somewhere in the 10^{-1} to 10^{1} torr range). This form of plasma discharge could cause permanent damage to the electronics of the BEA. There are two expected environments where this is applicable – thermal vacuum testing and in-flight operations.

The responsibility for correct operation of the high voltage control must fall on the Test Conductor. It should not be assumed that test scripts can be relied on to autonomously protect the instrument. Additionally, the concerns with high voltage operations may not be obvious to those unfamiliar with the operation of the ACD.

Sample HVBS Power-Up Sequence:

The following represents a strawman sequence of steps for correctly powering up a BEA HVBS. It is possible this might be used to form a template that could be used for an actual script.

1. Verify that the ACD +3.3V power is on and currents are nominal.
2. Verify that the BEA chassis is in the proper pressure environment (as described above).
3. Send an ACD GARC_Mode Read command. Verify bits [6:1] are 0.
4. Send an ACD GARC_Status Read command. Verify bits [2:1] are 0.
5. Verify that the ACD +28V power is on and currents are nominal.
6. Verify the GASU HVBS Monitors 1 and 2 are reading ~ 0V.
7. Send an ACD GARC_Mode write command with bits [3:1] at b'111.
8. Send an ACD GARC_Mode read command to verify this command.
9. Send an ACD GARC_Status Read command. Verify bits [2:1] are b'01, indicating HVBS 1 is enabled and HVBS 2 is disabled.
10. Send the GARC HVBS Level Write command with a data argument of 300. Verify with a GARC Read command.
11. Send the Use_HV_Normal write command. Verify the DAC register contents with the Use_HV_Normal read command.
12. Verify that the GASU HVBS Monitor 1 reads an equivalent of approximately 100V and that HVBS Monitor 2 reads approximately 0V. Verify that no phototube has a rate in excess of 1 kHz (if it does, stop at this point and inform the science team).
13. Verify that the +28V current is at a nominal value.
14. Repeat steps 10 – 13 with data arguments of 600, 900, 1200, etc. up to 3000. At a DAC register content of 3000, the HVBS should be at about 1000V. PMT rates should be less than 1 kHz.

Powering down the supply would be essentially the same sequence of steps, but in reverse (larger data argument steps could be used, for example steps of 1000). The DAC register would be ramped down to 0 and then the GARC_Mode enable bits would be zeroed out.